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09/836,104	04/17/2001	Yu-chun Chow	DEE-PT017	5930

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SILICON VALLEY PATENT GROUP LLP
2350 MISSION COLLEGE BOULEVARD
SUITE 360
SANTA CLARA, CA 95054

EXAMINER	
GREY, CHRISTOPHER P	

ART UNIT	PAPER NUMBER
2667	

DATE MAILED: 05/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/836,104	CHOW, YU-CHUN	
	Examiner	Art Unit	
	Christopher P Grey	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09836104.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. **The text of those sections of Title, U.S. Code not included in this action can be found in the prior Office action.**

2. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Konishi et al. (U.S Patent No. 5854792) in view of Merchant et al. (Patent No. 6658015)

Regarding claim 1, Konishi et al. (U.S Patent No. 5854792) teaches a gateway apparatus for using in performing communication between wide area networks (WAN) to local area networks (LAN), comprising:

a plurality of input/output ports for connecting said WAN with said LAN(see elements 5a, 5b and 5n in fig 3)

a buffer device for accessing packets(see element 17a-n in Fig 8), wherein a transporting path of said packets is selected from one of sending said packets from said WAN to said LAN and sending said packets from said LAN to said WAN(disclosed in Col 8 lines 53-57),

a memory device(see element 9 in fig 3) electrically connected to said buffer device for storing said packets sent from said buffer device,

However, Konishi et al. (U.S Patent No. 5854792) does not teach a plurality of medium access control units corresponding to said input/output ports and, electrically connected between said buffer device and said input/output ports for performing an accessing operation between said buffer device and said input/output ports.

Konishi et al. (U.S Patent No. 5854792) also does not teach a central processing unit electrically connected between said memory device and said medium access control units for processing said packets stored in said memory device, and organizing said medium access control units to change said input/output ports according to a required transporting path , thereby performing said communication between said LAN and said WAN.

The secondary reference Merchant et al. (Patent No. 6658015) teaches a plurality of medium access control units(see element 20 in Fig 1) corresponding to said input/output ports and, electrically connected between said buffer device and said input/output ports for performing an accessing operation between said buffer device and said input/output ports, as disclosed in Col 5 lines 6-15.

The secondary reference Merchant et al. (Patent No. 6658015) also teaches a central processing unit (see element 32 in Fig 1) electrically connected between said memory device and said medium access control units for processing said packets stored in said memory device, and organizing said medium access control units to change said input/output ports according to a required transporting path , thereby performing said communication between said LAN and said WAN, as disclosed in Col 10 lines1-5.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the ports within the network connection apparatus as disclosed by Konisha, with the connection of a MAC module, CPU and internal rules checker as disclosed by Merchant. The motivation for this modification is to be able to receive and

transmit data frames to the appropriate destinations (Col 1 lines 22-27), support data networks requiring a high data throughput (Col 1 lines 65-67), and to allow multiple frames to be processed simultaneously (Col 2 lines 5-9).

Regarding claim 2, the primary reference Konishi et al. (U.S Patent No. 5854792) teaches all of the limitations as mentioned above. However, the primary reference does not teach the gateway apparatus according to claim 1, wherein said buffer device comprises: a buffer for temporally storing said packets, and a buffer manager electrically connected to said buffer for managing an accessing operation of said buffer device.

The secondary reference Merchant et al. (Patent No. 6658015) teaches a gateway apparatus, wherein said buffer device comprises: a buffer for temporally storing said packets and a buffer manager electrically connected to said buffer for managing an accessing operation of said buffer device, as disclosed in Col 5 lines 5-15.

Regarding claim 3, the primary reference Konishi et al. (U.S Patent No. 5854792) teaches all of the limitations as mentioned above. However, the primary reference does not teach the gateway apparatus according to claim 1, wherein said memory device comprises:

a memory for storing said packets sent from said buffer device and a memory controller electrically connected to said memory for controlling an accessing operation of said memory.

The secondary reference Merchant et al. (Patent No. 6658015) teaches a gateway apparatus, wherein said memory device comprises:

a memory for storing said packets (see element 44 in Fig 2) sent from said buffer device and a memory controller (see element 80 in Fig 3a) electrically connected to said memory for controlling an accessing operation of said memory, as disclosed in Col 6 lines 52-63.

Regarding claim 4, the primary reference Konishi et al. (U.S Patent No. 5854792) teaches all of the limitations as mentioned above. However, the primary reference does not teach the gateway apparatus according to claim 3, wherein said memory is a dynamic random accessing memory DRAM.

The secondary reference Merchant et al. (Patent No. 6658015) teaches a gateway apparatus, wherein said memory is a dynamic random accessing memory DRAM (see element 44 in Fig 2), as disclosed in Col 4 lines 35-45, where the limitations for an SRAM are assumed to be equivalent for that of a DRAM.

Regarding claim 5, the primary reference Konishi et al. (U.S Patent No. 5854792) teaches all of the limitations as mentioned above. However, the primary reference does not teach the gateway apparatus according to claim 3, further comprising:

an internal bus electrically connected to said memory controller for transporting said packets

a bus interface controller electrically connected between said buffer device and said internal bus for controlling a transporting operation in said internal bus so as to complete a packet transporting operation between said buffer device and said internal bus.

The secondary reference Merchant et al. (Patent No. 6658015) teaches a gateway apparatus, comprising:

an internal bus (see element 69 in Fig 2) electrically connected to said memory controller for transporting said packets (disclosed in Col 6 line 64- Col 7 line15)

a bus interface controller (see element 40 in Fig 2)electrically connected between said buffer device and said internal bus for controlling a transporting operation in said internal bus so as to complete a packet transporting operation between said buffer device and said internal bus as disclosed in Col 5 lines 16-40.

Regarding claim 6, the primary reference Konishi et al. (U.S Patent No. 5854792) teaches all of the limitations as mentioned above. However, the primary reference does not teach the gateway apparatus according to claim 1, wherein said buffer device, said

medium access control units and said central processing unit are disposed in one identical chip.

The secondary reference Merchant et al. (Patent No. 6658015) teaches a gateway apparatus, wherein said buffer device, said medium access control units (see element 12a in Fig 1) and said central processing unit (see element 32 in fig 1) are disposed in one identical chip.

Regarding claim 7, the primary reference Konishi et al. (U.S Patent No. 5854792) teaches all of the limitations as mentioned above. However, the primary reference does not teach the gateway apparatus according to claim 1, wherein said central processing unit is used for processing said packets stored in said memory device to achieve functions of a router and a firewall.

The secondary reference Merchant et al. (Patent No. 6658015) teaches a gateway apparatus, wherein said central processing unit is used for processing said packets stored in said memory device to achieve functions of a router and a firewall, as disclosed in Col 4 lines 52-59.

It would have been obvious for one skilled in the art at the time to combine the ideas of Konishi et al. (U.S Patent No. 5854792) and Merchant et al. (Patent No. 6658015) in order to achieve a general purpose network connection apparatus capable of increased data throughput, performing high speed data transmission and enhancing the reliability of transmission.

Drawings

3. The amended drawings are objected to for the following reason:

(a) The 'prior art' label is handwritten

Appropriate correction is required

Response to Arguments

4. Applicant's arguments filed on December 10, 2004 have been fully considered but they are not persuasive.

Claim 1

(a) The applicant argued that the cited art does not disclose Applicant's claimed "plurality of input/output ports for connecting said WAN with said LAN".

The examiner maintains that the same limitation, in its broadest term, is already discussed in the rejection of claim 1, wherein Konisha discloses a number of signal lines/links (elements 5 a-n in Figs 1 and 3, and Col 5 lines 5-10) connecting a number of LAN's or WAN's together, where inherently, the links are connected end-to-end via ports. Furthermore, it would have been obvious to one of the ordinary skill in the art at the time of the invention to interpret the network-to-network connection as disclosed by Konisha, as a LAN to WAN connection.

(b) The applicant argued that the cited art does not disclose Applicant's claimed "changing input/output ports according to a required transporting path, thereby performing said communication between sad LAN and said WAN".

The examiner maintains that the same limitation, in its broadest term, is already discussed in the rejection of claim 1, wherein Konisha discloses a route control section, which designates the destination and sender network (path) of the transmission frame (Col 10 lines 4-16). Furthermore it would have been obvious to one of the ordinary skill in the art at the time of the invention that any route control device operates to control the path/route selected for transmission of data. Furthermore, it would have been obvious that controlling (changing) the route would involve controlling the links (ports) disclosed in the response to arguments of claim 1.

(c) The applicant argued that the cited art does not disclose Applicant's claimed "buffer device".

The examiner maintains that the same limitation, in its broadest term, is already discussed in the rejection of claim 1, wherein Konisha discloses a number of buffer devices (elements 17 a-n) for receiving data (Col 7 lines 47-51). Furthermore it would have been obvious to one of the ordinary skill in the art at the time of the invention to equivocate any of the buffers as disclosed by Konisha to the buffer device disclosed in claim 1.

(d) The applicant argued that the cited art does not disclose Applicant's claimed "processing packets stored in the memory device, and organizing the medium access units to change the input/output ports according to a required transporting path".

The examiner maintains that the same limitation, in its broadest term, is already discussed in the rejection of claim 1, wherein Merchant discloses a CPU (Col 10 lines 1-5) connected to an internal rules checker (IRC) which includes an address table

(memory) as disclosed in Col 9 lines 15-31. Merchant also discloses the IRC storing frames and processing the frames in an efficient manner (Col 8 line 57– Col 9 lines 15). Merchant also discloses the CPU being connected to a management MAC unit (Col 10 lines1-5). Merchant discloses the IRC making forwarding decisions that involve assigning a port (Col 11 lines 12-36).

(e) In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, it would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the ports within the network connection apparatus as disclosed by Konisha, with the connection of a MAC module, CPU and internal rules checker as disclosed by Merchant. The motivation for this modification is to be able to receive and transmit data frames to the appropriate destinations (Col 1 lines 22-27), support data networks requiring a high data throughput (Col 1 lines 65-67), and to allow multiple frames to be processed simultaneously (Col 2 lines 5-9).

Claims 2-7

(a) The rejection of Claims 2-7 remains unchanged as they are dependent on claim 1.

Conclusion

5. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher P Grey whose telephone number is (571)272-3160. The examiner can normally be reached on 6:30-3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (571)272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher Grey
Examiner
Art Unit 2667

5/2/05

CHI PHAM
SUPERVISORY PATENT EXAMINE
TECHNOLOGY CENTER 2600

5/5/05